WHAT IS CLAIMED IS:

1. An amplifier, comprising:

an input stage configured to receive an amplifier input signal;

a plurality of output stages configured to combinatorially produce an amplifier output; and

an output stage controller coupled to the input stage and the output stages;

wherein each of the plurality of output stages is configured to receive a supply voltage that is different from any other output stage;

wherein each of the plurality of output stages comprises an output transistor, and

wherein in response to the amplifier input signal, the output stage controller is configured to generate control signals that cause each of the plurality of output stages to contribute current to the output of the amplifier when the output of the amplifier is less than the supply voltage received by the output stage.

2. The amplifier of claim 1 configured as a class G amplifier.

3. The amplifier of claim 1, wherein the maximum output voltage of the amplifier is equal to a highest supply voltage minus the product of the amplifier output current and Rdson for the output transistor comprised in the one of the plurality of output stages associated with the highest supply voltage.

4. The amplifier of claim 1, wherein the Rdson for the output transistors is inversely proportional to the channel width of the transistors.

5. The amplifier of claim 1, wherein the product of the amplifier output current and Rdson for the output transistor comprised in the one of the plurality of output stages associated with the highest supply voltage is approximately 0.15V.

6. The amplifier as recited in claim 1, wherein for each of the plurality of output stages except for the one of the plurality of output stages configured to receive a highest supply voltage, the output stage controller is configured to generate a control signal, which changes state in response to the amplifier output voltage reaching the voltage level of the supply voltage received by the output stage.

7. The amplifier as recited in claim 6, wherein each of the control signals controls an analog switch coupled between an input and output of the corresponding output stage, wherein if the amplifier output is increasing, the control signal is configured to close the analog switch, wherein if the amplifier output is decreasing, the control signal is configured to open the analog switch.

8. The amplifier as recited in claim 7, wherein when the analog switch is closed the output transistor comprised in the output stage is configured to inhibit current from flowing from the amplifier output into a power supply associated with the output stage.

9. The amplifier as recited in claim 7, wherein when the analog switch is open the output transistor comprised in the output stage is configured to allow current to flow from a power supply associated with the output stage to the amplifier output.

10. The amplifier as recited in claim 1 implemented as an integrated circuit using CMOS technology.

11. The amplifier as recited in claim 1 configured to drive a fan.

12. The amplifier as recited in claim 1, wherein each of the plurality of output stages is configured to provide a voltage gain greater than unity.

13. A class G amplifier, wherein when the amplifier output voltage is in a range between the supply voltage received by an output stage and a voltage differential, delta V, below said supply voltage, both that output stage and another output stage receiving a next higher supply voltage contribute current to the amplifier output.

14. The class G amplifier as recited in claim 13, wherein delta V is determined by the W/L ratio of transistors comprised in the output stage controller.

15. The class G amplifier as recited in claim 13, wherein delta V is in the range of 0V to 0.8V.

16. The class G amplifier as recited in claim 13, wherein delta V is approximately 0.3V.

17. A class G amplifier, wherein each of the plurality of output stages, except for an output stage configured to receive a lowest supply voltage, is configured to contribute current to the amplifier output when the amplifier output voltage is in a range from the supply voltage received by that output stage to a next lower supply voltage less a differential voltage, delta V.

18. The class G amplifier as recited in claim 17, wherein the output stage associated with the lowest supply voltage is configured to contribute current to the amplifier output when the amplifier output voltage is in a range from 0V, to the lowest supply voltage.

19. The class G amplifier as recited in claim 17, wherein delta V is in a range of 0V to approximately 0.8V.

20. The class G amplifier as recited in claim 17, wherein delta V is approximately 0.3V

21. A method comprising:

outputting current from an output stage associated with a lowest supply voltage when an amplifier output voltage is less than the lowest supply voltage;

outputting current from an output stage associated with a highest supply voltage when the amplifier output voltage is greater than the next lower supply voltage minus delta V; and

outputting current from an output stage associated with a supply voltage other than the lowest or highest supply voltage when the amplifier output voltage is between a next lower supply voltage minus delta V, and the supply voltage associated with that output stage.

22. The method of claim 21, wherein delta V is determined by the W/L ratio of transistors comprised in an output stage controller.

23. The method of claim 21, wherein delta V is in the range of 0V to 0.8V.

24. The method of claim 21, wherein delta V is approximately 0.3V.

25. The method of claim 21, wherein the number of output stages and corresponding supply voltages is greater than 3.

26. The method of claim 21, wherein the maximum output voltage of the amplifier is equal to a highest supply voltage minus the product of the amplifier output current and Rdson for the output transistor comprised in the one of the plurality of output stages associated with the highest supply voltage.

27. The method of claim 21, wherein the product of the amplifier output current and Rdson for the output transistor comprised in the one of the plurality of output stages associated with the highest supply voltage is approximately 0.15V.

28. The method of claim 21, further comprising isolating the output of each output stage from the amplifier output voltage when the amplifier output voltage is greater than the supply voltage associated with that output stage.

29. A method comprising:

generating a first current that is inversely proportional to an output voltage of an amplifier;

generating a second current that is directly proportional to a sum of currents output by the output stages of the amplifier;

combining the first and second currents such that under normal amplifier operation the resulting current is constant and less than a limiting value, Ilim, for a range of output voltages for the amplifier.

30. The method of claim 29, wherein the combined first and second currents control a resistance between an input voltage of the amplifier and ground.

31. The method of claim 30, further comprising reducing the resistance between the input voltage of the amplifier and ground in response to the value of the combined first and second currents exceeding Ilim.

32. The method of claim 31, wherein the reduction in resistance between the input voltage of the amplifier and ground is proportional to the amount by which the combined first and second currents exceed Ilim.